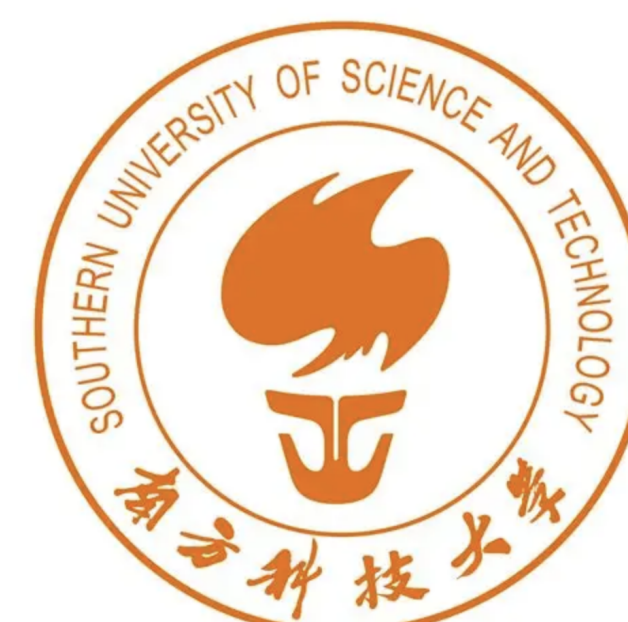




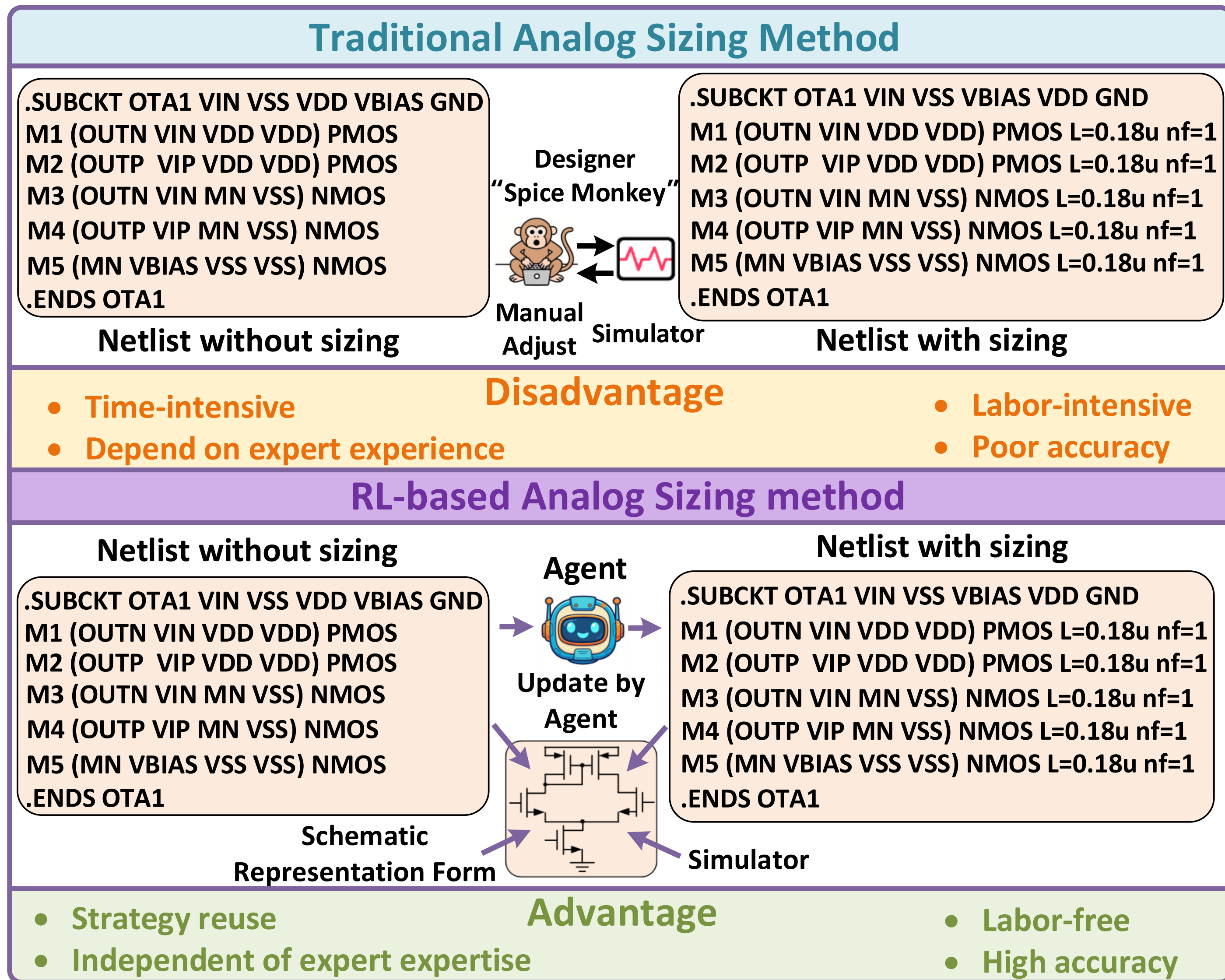
FD-MAGRPO: Functionality-Driven Multi-Agent Group Relative Policy Optimization for Analog-LDO Sizing

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Background and Motivation

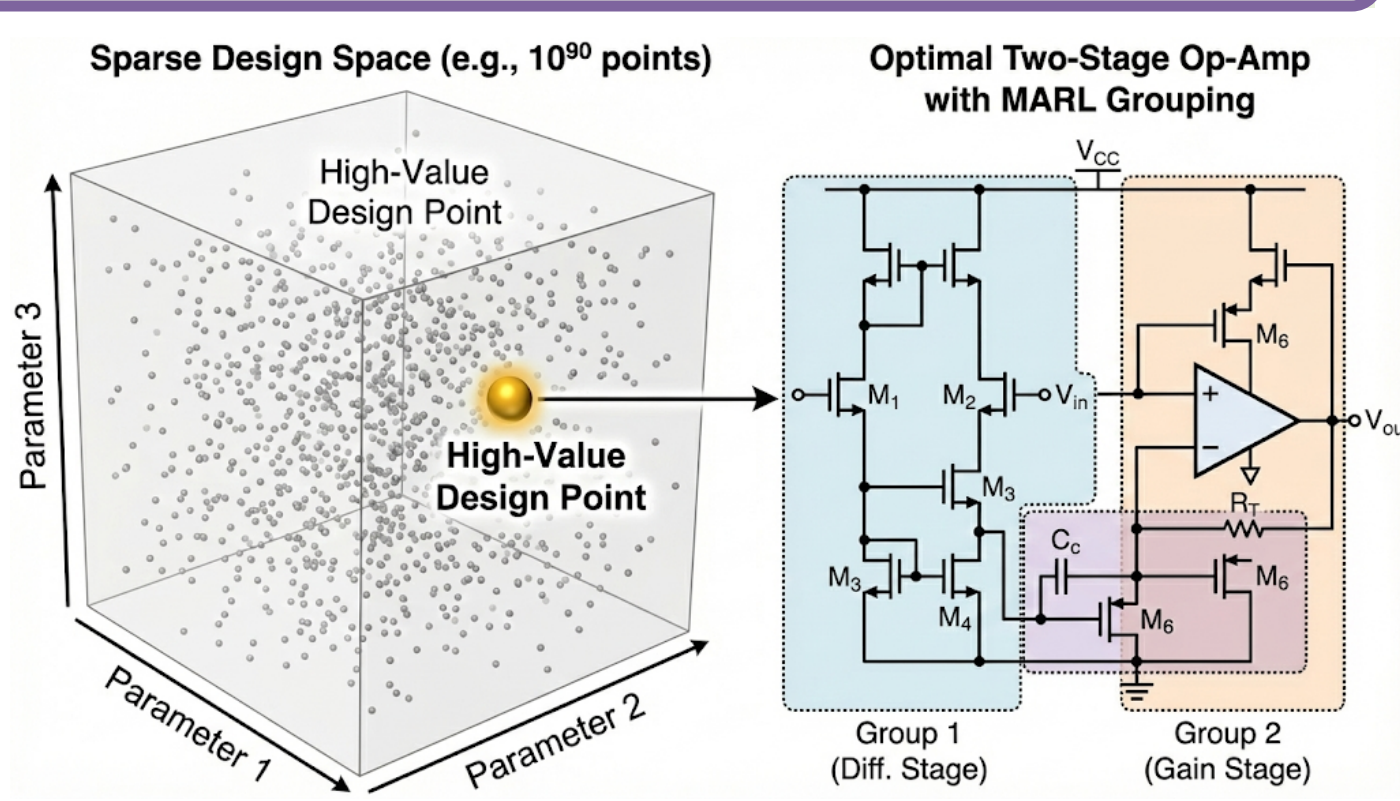


Challenges in Analog Circuit Sizing:

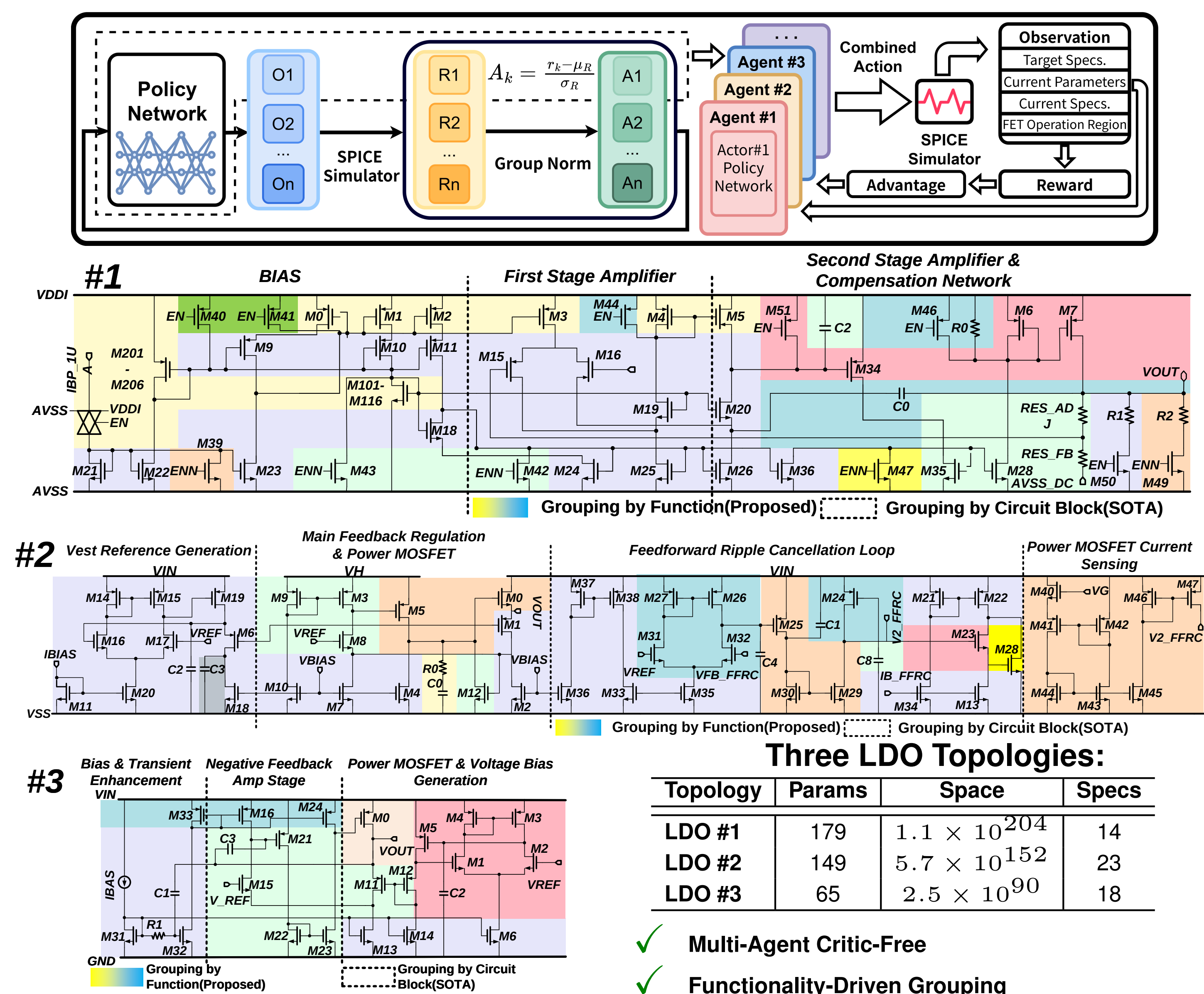
- Massive design space: 10^{90} – 10^{204}
- Sparse rewards from SPICE

Limitations of Existing MARL Methods:

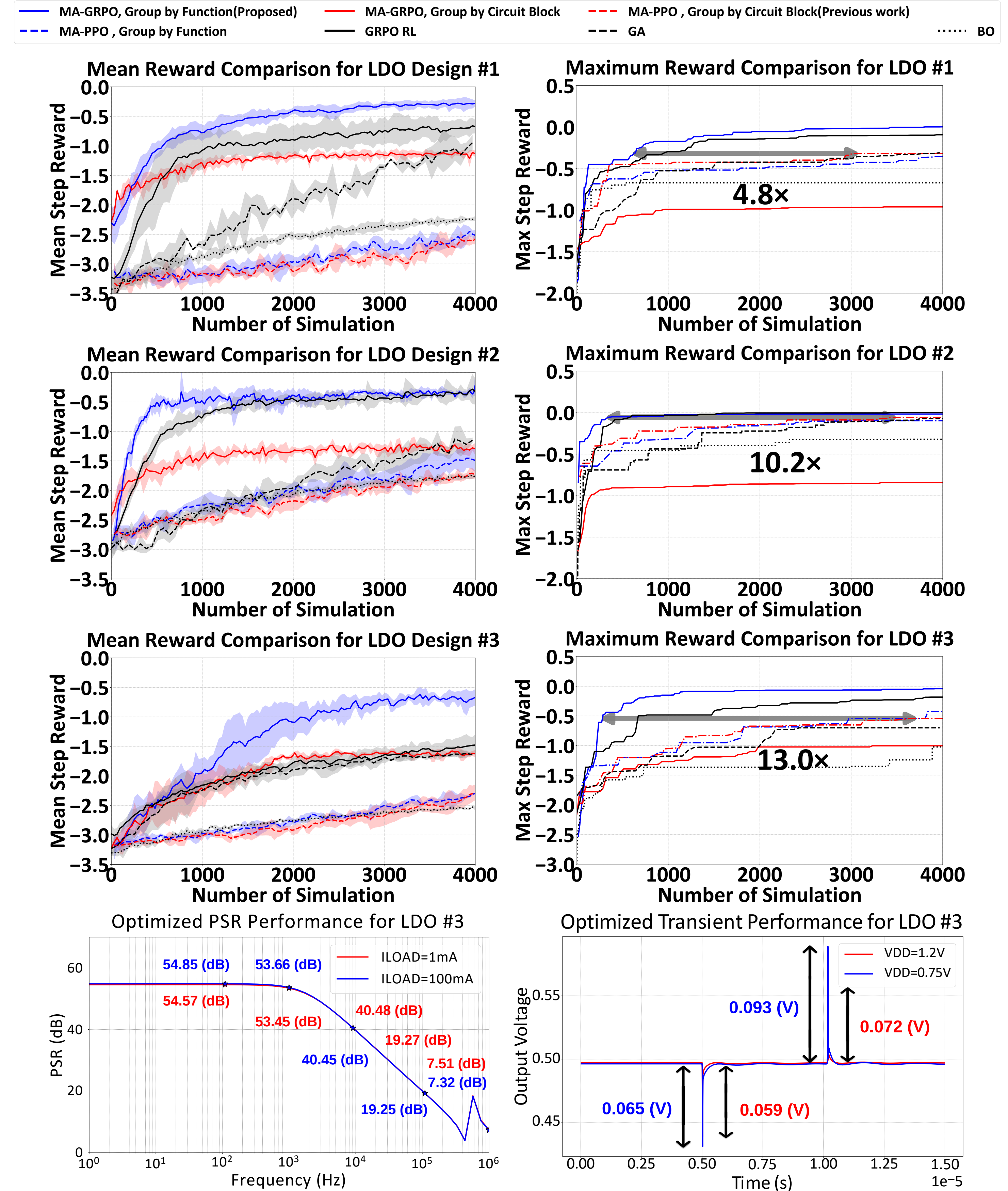
- Critic networks fail in sparse rewards
- Block grouping ignores functional dependencies



Proposed FD-MAGRPO Framework



Experimental Results & Validation



Specification	Reported	Optimized	Improv.
IQ(μ A)	8.00	7.91	1%
Line Reg. ¹ (mV/V)	4.50	1.80	60%
Line Reg. ² (mV/V)	7.80	1.96	75%
Load Reg.(V/A)	0.12	0.002	98%
Overshoot ³ (V)	0.11	0.092	16%
Undershoot ³ (V)	0.077	0.065	16%
Overshoot ⁴ (V)	0.072	0.072	0%
Undershoot ⁴ (V)	0.062	0.059	5%
PSR@100Hz ² (dB)	51.0	54.9	8%
PSR@1kHz ² (dB)	45.0	53.7	19%
PSR@10kHz ² (dB)	25.0	40.5	62%
PSR@100kHz ² (dB)	3.0	19.3	542%
PSR@1MHz ² (dB)	0	7.3	∞
PSR@100Hz ¹ (dB)	50.0	54.6	9%
PSR@1kHz ¹ (dB)	45.0	53.5	19%
PSR@10kHz ¹ (dB)	25.0	40.5	62%
PSR@100kHz ¹ (dB)	5.0	19.3	285%
PSR@1MHz ¹ (dB)	0	7.5	∞
FoM(fFV/A)	0.588	0.581	1%

¹I_{LOAD}=1mA, ²I_{LOAD}=100mA, ³VDD=0.75V, ⁴VDD=1.2V

$$\text{FoM: FoM} = \frac{I_Q C_L \Delta V_{OUT}}{\Delta I_{LOAD}^2}$$

Gradient SNR Comparison (Functionality vs. Block):

Step	LDO #1				LDO #2				LDO #3			
	Func.-based	Block-based	Func.-based	Block-based	Func.-based	Block-based	Func.-based	Block-based	Func.-based	Block-based	Func.-based	Block-based
1	0.222	0.211	0.199	0.197	0.227	0.219	0.221	0.208	0.232	0.224	0.197	0.189
5	0.198	0.186	0.171	0.168	0.223	0.216	0.202	0.202	0.198	0.196	0.148	0.145
10	0.248	0.247	0.214	0.208	0.225	0.220	0.199	0.197	0.224	0.219	0.220	0.214
20	0.293	0.272	0.217	0.205	0.245	0.239	0.194	0.190	0.244	0.238	0.209	0.203
40	0.296	0.283	0.205	0.186	0.215	0.209	0.204	0.187	0.226	0.219	0.187	0.184

Note: $\overline{\text{GSNR}}_h$ denotes harmonic mean GSNR. Functionality-based grouping achieves consistently higher GSNR $\Rightarrow$ clearer credit assignment $\Rightarrow$ faster convergence.

Key Achievements:

- Rapid convergence:** 800–3000 simulations across three LDO topologies
- Significant speedup:** 4.8x–13.0x faster than SOTA RL methods
- Scalability:** Optimizes circuits with up to 179 parameters in 10^{204} design space

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